High Efficiency Synchronous Step-Down Switching Regulators

ADP1148, ADP1148-3.3, ADP1148-5

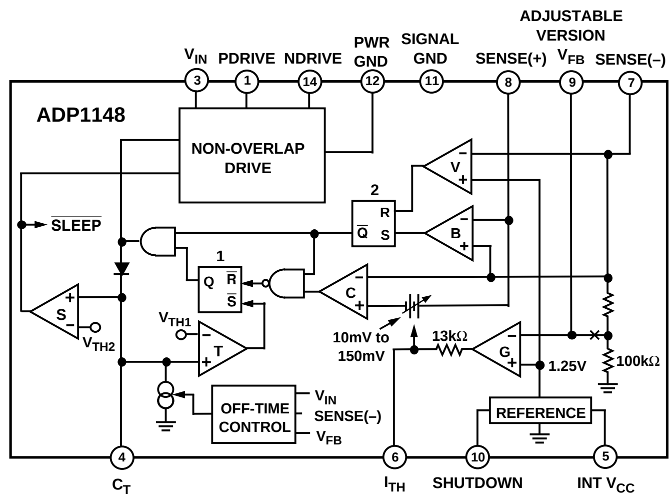
FEATURES

Operation From 3.5 V to 18 V Input Voltage
Ultra High Efficiency > 95%
Low Shutdown Current
Current Mode Operation for Excellent Line & Load Transient Response
High Efficiency Maintained Over Wide Current Range
Logic Controlled Micropower Shutdown
Short Circuit Protection
Very Low Dropout Operation
Synchronous FET Switching for High Efficiency
Adaptive Nonoverlap Gate Drives

APPLICATIONS

Notebook and Palmtop Computers
Portable Instruments
Battery Operated Digital Devices
Industrial Power Distribution
Avionics Systems
Telecom Power Supplies
GPS Systems
Cellular Telephones

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP1148 is part of a family of synchronous step-down switching regulator controllers featuring automatic sleep mode to maintain high efficiencies at low output currents. These devices drive external complementary power MOSFETs at switching frequencies up to 250 kHz using a constant off-time current-mode architecture.

The constant off-time architecture maintains constant ripple current in the inductor, easing the design of wide input range converters. Current-mode operation provides excellent line and load transient response. The operating current level is user programmable via an external current sense resistor.

The ADP1148 incorporates automatic Power Saving Sleep Mode operation when load currents drop below the level required for continuous operation. In sleep mode, standby power is reduced to only about 2 mW at V_{IN} = 10 V. In shutdown, both MOSFETs are turned off.

TYPICAL APPLICATIONS

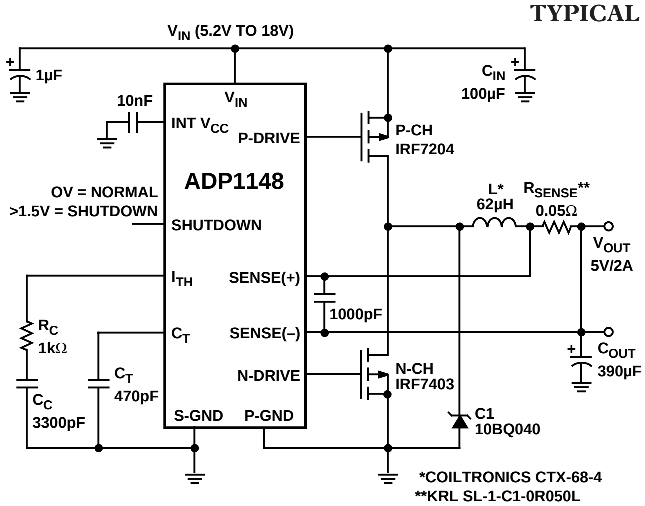


Figure 1. High Efficiency Step-Down Converter

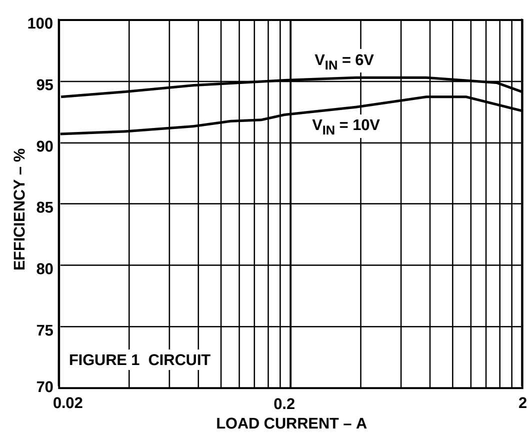


Figure 2. ADP1148-5 Typical Efficiency

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 World Wide Web Site: http://www.analog.com
Fax: 617/326-8703

ADP1148, ADP1148-3.3, ADP1148-5–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ +70°C,[1] V_{IN} = 10 V, $V_{SHUTDOWN}$ = 0 V, unless otherwise noted. See Figure 17.)

Parameter	Symbol	Conditions[2]	Min	Typ	Max	Units
FEEDBACK VOLTAGE ADP1148 Only	V_{10}	V_{IN} = 9 V	1.21	1.25	1.29	V
FEEDBACK CURRENT ADP1148 Only	I_{10}			0.2	1.0	μA
REGULATED OUTPUT VOLTAGE	V_{OUT}	V_{IN} = 9 V				
ADP1148–3.3		I_{LOAD} = 700 mA	3.23	3.33	3.43	V
ADP1148–5		I_{LOAD} = 700 mA	4.9	5.05	5.2	V
OUTPUT VOLTAGE LINE REGULATION	dV_{OUT}	T_A = +25°C, V_{IN} = 7 V to 12 V, I_{LOAD} = 50 mA	–40		+40	mV
OUTPUT VOLTAGE LOAD REGULATION	dV_{OUT}					
ADP1148–3.3		5 mA < I_{LOAD} < 2 A		40	65	mV
ADP1148–5		5 mA < I_{LOAD} < 2 A		60	100	mV
SLEEP MODE OUTPUT RIPPLE	dV_{OUT}	I_{LOAD} = 0 A		50		mV p-p
INPUT DC SUPPLY CURRENT[3]	I_Q	T_A = +25°C				
Normal Mode		V_{IN} = 4 V < V_{IN} < 18 V		1.6	2.3	mA
Sleep Mode (ADP1148–3.3)		V_{IN} = 4 V < V_{IN} < 18 V		160	250	μA
Sleep Mode (ADP1148–5)		V_{IN} = 4 V < V_{IN} < 18 V		160	250	μA
Shutdown		$V_{SHUTDOWN}$ = 2.1 V, 4 V < V_{IN} < 15 V		10	20	μA
CURRENT SENSE THRESHOLD VOLTAGE[4]	$V_8–V_7$	V_9 = V_{OUT}/4 + 25 mV (Forced), V_8 = 5 V, T_A = +25°C		25		mV
ADP1148 Only		V_9 = V_{OUT}/4 mV – 25 mV (Forced), V_8 = 5 V,	130	150	170	mV
ADP1148–3.3		$V_{SENSE}(–)$ = V_{OUT} + 100 mV (Forced), T_A = +25°C		25		mV
		$V_{SENSE}(–)$ = V_{OUT} – 100 mV (Forced)	130	150	170	mV
ADP1148–5		$V_{SENSE}(–)$ = V_{OUT} + 100 mV (Forced) T_A = +25°C		25		mV
		$V_{SENSE}(–)$ = V_{OUT} – 100 mV (Forced)	130	150	170	mV
SHUTDOWN PIN THRESHOLD ADP1148-3.3, ADP1148-5	V_{10}	T_A = +25°C	0.6	0.8	2.0	V
SHUTDOWN PIN INPUT CURRENT	I_{10}	0 V < $V_{SHUTDOWN}$ < 8 V, V_{IN} = 18 V		1.2	5	μA
C_T PIN DISCHARGE CURRENT	I_4	T_A = +25°C, V_{OUT} in Regulation, $V_{SENSE}(–)$ = V_{OUT},	50	65	90	μA
		V_{OUT} = 0 V		2	10	μA
OFF-TIME	t_{OFF}	C_T = 390 pF, I_{LOAD} = 700 mA	4	5	6	μs
DRIVER OUTPUT TRANSITION TIMES	t_R, t_F	C_L = 3000 pF (Pins 1, 14) V_{IN} = 6 V, T_A = +25°C		100	200	ns

NOTES

[1]All limits at temperature extremes are guaranteed via correlation using standard Quality Control methods. Specifications subject to change without notice.

[2]T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

ADP1148AR, ADP1148AR–3.3, ADP1148AR–5: $T_J = T_A + (P_D \times 110°C/W)$

ADP1148AN, ADP1148AN–3.3, ADP1148AN–5: $T_J = T_A + (P_D \times 70°C/W)$

[3]Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. The allowable operating frequency may be limited by power dissipation at high input voltages.

[4]The ADP1148 version is tested with external feedback resistors, setting the nominal output voltage to 5 V.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (–40°C ≤ T_A ≤ +85°C,[1] V_{IN} = 10 V, $V_{SHUTDOWN}$ = 0 V, unless otherwise noted. See Figure 17.)

Parameter	Symbol	Conditions[2]	Min	Typ	Max	Units
FEEDBACK VOLTAGE						
ADP1148 Only	V_{10}	V_{IN} = 9 V	1.20	1.25	1.30	V
REGULATED OUTPUT VOLTAGE	V_{OUT}	V_{IN} = 9 V				
ADP1148-3.3		I_{LOAD} = 700 mA	3.17	3.33	3.4	V
ADP1148-5		I_{LOAD} = 700 mA	4.85	5.05	5.2	V
INPUT DC SUPPLY CURRENT[3]	I_Q					
Normal Mode		V_{IN} = 4 V < V_{IN} < 18 V		1.6	2.6	mA
Sleep Mode (ADP1148-3)		V_{IN} = 4 V < V_{IN} < 18 V		160	280	µA
Sleep Mode (ADP1148-5)		V_{IN} = 6 V < V_{IN} < 18 V		160	280	µA
Shutdown		$V_{SHUTDOWN}$ = 2.1 V, 4 V < V_{IN} < 12 V		10	24	µA
CURRENT SENSE THRESHOLD VOLTAGE[4]	V_8–V_7					
ADP1148 Only		V_9 = V_{OUT}/4 + 25 mV (Forced), V_8 = 5 V		10		mV
		V_9 = V_{OUT}/4 – 25 mV (Forced), V_8 = 5 V	115	150	175	mV
ADP1148-3.3		V_{SENSE} = V_{OUT} + 100 mV (Forced)		25		mV
		V_{SENSE} = V_{OUT} – 100 mV (Forced)	115	150	175	mV
ADP1148-5.0		V_{SENSE} = V_{OUT} + 100 mV (Forced)		25		mV
		V_{SENSE} = V_{OUT} – 100 mV (Forced)	115	150	175	mV
SHUTDOWN PIN THRESHOLD	V_{10}					
ADP1148-3.3, ADP1148-5			0.55	0.8	2	V
OFF-TIME	t_{OFF}	C_T = 390 pF, I_{LOAD} = 700 mA	4	5	6.2	µs

NOTES
[1]All limits at temperature extremes are guaranteed via correlation using standard Quality Control method.
[2]T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:
ADP1148AR, ADP1148AR-3, ADP1148AR-5: $T_J = T_A + (P_D \times 110°C/W)$
ADP1148AN, ADP1148AN-3, ADP1148AN-5: $T_J = T_A + (P_D \times 70°C/W)$
[3]Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. The allowable operating frequency may be limited by power dissipation at high input voltages.
[4]The ADP1148 version is tested with external feedback resistors setting the nominal output voltage to 5 V.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (Pin 3) . . . . –0.3 V to +20 V
Continuous Output Currents (Pins 1, 14) . . . . 50 mA
Sense Voltages (Pins 7, 8) . . . . –0.3 V to V_{CC}
Operating Temperature Range . . . . 0°C to +70°C
Extended Commercial Temperature Range . . –40°C to +85°C
Junction Temperature[1] . . . . 150 °C
Storage Temperature Range . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . 300°C

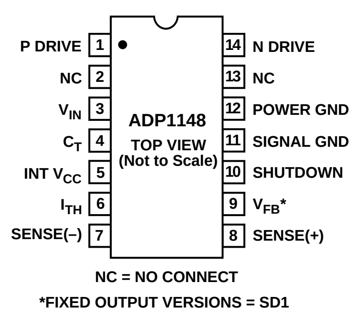
ORDERING GUIDE

Model	Output Voltage	Package Description	Package Option
ADP1148AN	ADJ	Plastic DIP	N-14
ADP1148AR	ADJ	Small Outline Package	SO-14
ADP1148AN-3.3	3.3 V	Plastic DIP	N-14
ADP1148AR-3.3	3.3 V	Small Outline Package	SO-14
ADP1148AN-5	5 V	Plastic DIP	N-14
ADP1148AR-5	5 V	Small Outline Package	SO-14

PIN DESCRIPTION

Pin #	Mnemonic	Function
1	P-Channel Drive	High Current Gate Drive for Top P-Channel MOSFET. The voltage swing at Pin 4 is from V_{IN} to ground.
2	NC	No Connection.
3	V_{IN}	Input Voltage.
4	C_T	External Capacitor C_T from Pin 4 to Ground Sets the Operating Frequency. The frequency is also dependent on the ratio V_{OUT}/V_{IN}.
5	Int V_{CC}	Internal Supply Voltage, Nominally 3.3 V. Must be decoupled to signal ground. Do not externally load this pin.
6	I_{TH}	Error Amplifier Decoupling Point. The current comparator threshold increases with the Pin 7 voltage.
7	Sense–	Connects to internal resistive divider that sets the output voltage in ADP1148-3.3 and ADP1148-5 versions. Pin 7 is also the (–) input for the current comparator.
8	Sense+	The (+) Input for the Current Comparator. A built-in offset between Pins 7 and 8, in conjunction with R_{SENSE}, sets the current trip threshold.
9	V_{FB}	For the ADP1148 adjustable version, Pin 9 serves as the feedback pin from an external resistive divider used to set the output voltage. On ADP1148-3.3 and ADP1148-5 versions, this pin is not used.
10	Shutdown	Taking Pin 10 of the ADP1148, ADP1148-3.3 or ADP1148-5 high holds both MOSFETs off. Must be at ground potential for normal operation.
11	Signal GND	Small Signal Ground. Must be routed separately from other grounds to the (–) terminal of C_{OUT}.
12	Power GND	Driver Power Ground. Connects to source of N-channel MOSFET and the (–) terminal of C_{IN}.
13	NC	No Connection.
14	N-Channel Drive	High Current Drive for bottom N-channel MOSFET. The voltage swing at Pin 13 is from ground to V_{IN}.

PIN CONFIGURATIONS
14-Lead Plastic DIP
14-Lead Plastic SO



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP1148, ADP1148-3.3, ADP1148-5 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Typical Performance Characteristics–ADP1148, ADP1148-3.3, ADP1148-5

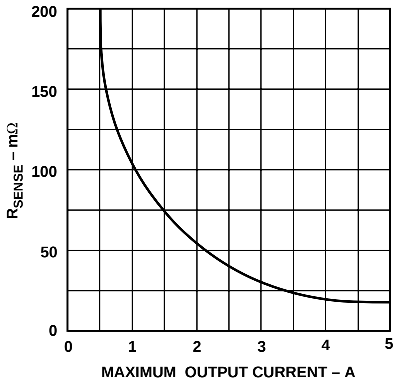


Figure 3. Selecting R_{SENSE} vs. Maximum Output Current

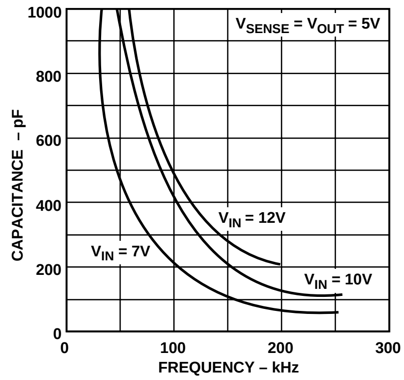


Figure 4. Operating Frequency vs. Timing Capacitor Value

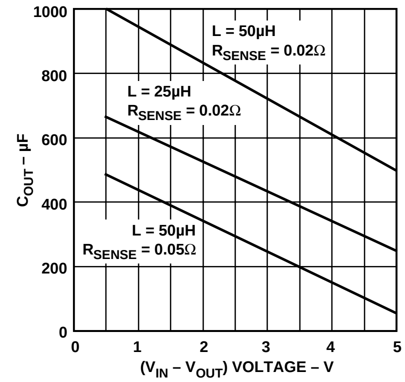


Figure 5. Selecting Minimum Output Capacitor vs. (V_{IN}–V_{OUT}) and Inductor

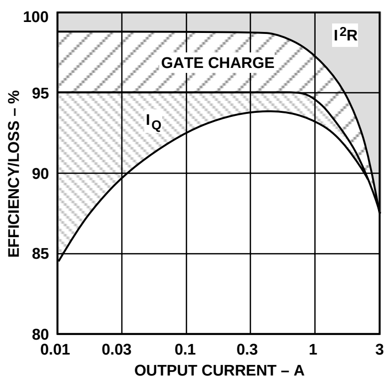


Figure 6. Typical Efficiency Losses

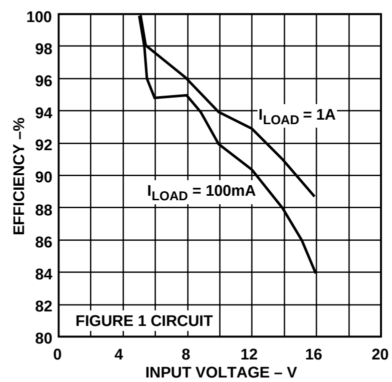


Figure 7. Efficiency vs. Input Voltage

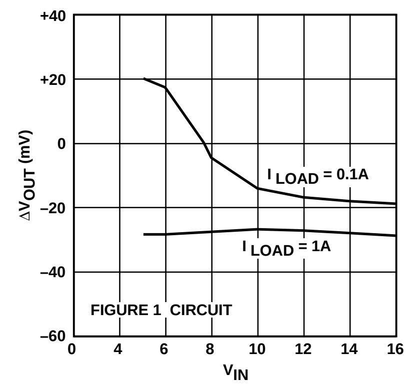


Figure 8. ADP1148-5 Output Voltage Change vs. Input Voltage

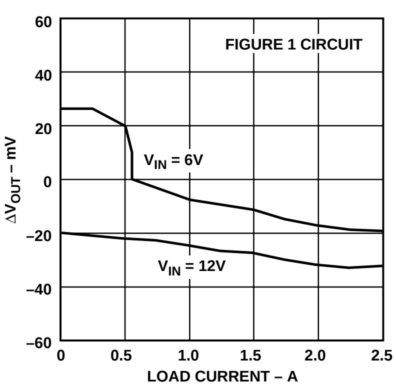


Figure 9. Load Regulation

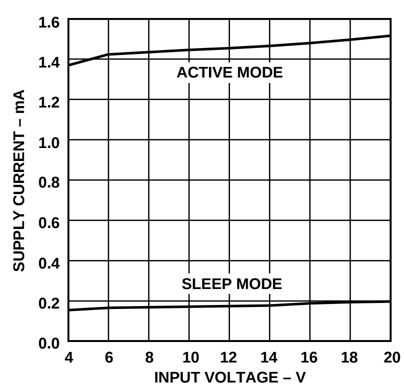


Figure 10. DC Supply Current

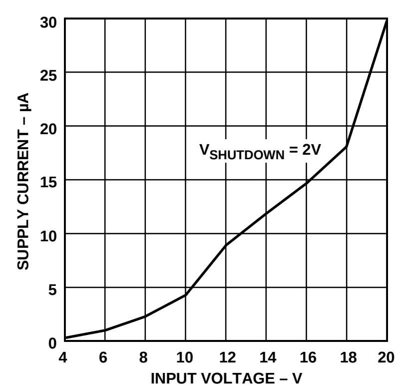


Figure 11. Supply Current in Shutdown

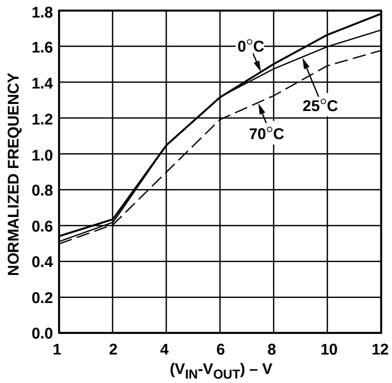


Figure 12. Operating Frequency vs. (V_{IN}–V_{OUT})

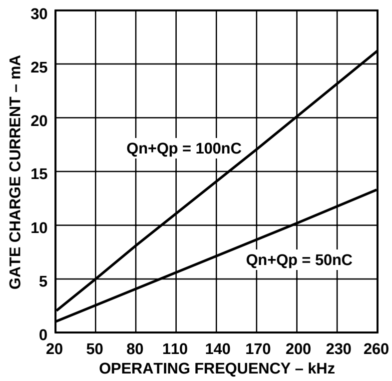


Figure 13. Gate Charge Supply Current

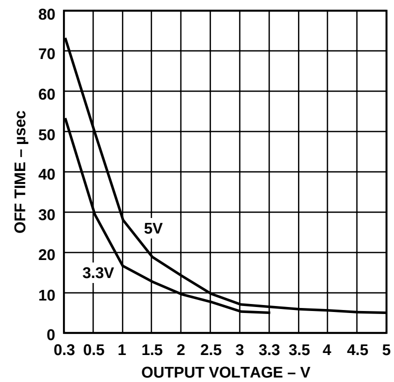


Figure 14. Off Time vs. V_{OUT}

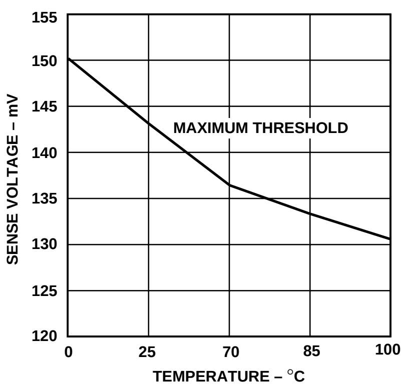


Figure 15. Current Sense Threshold Voltage

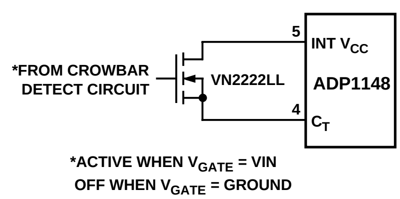


Figure 16. Output Crowbar Interface

APPLICATIONS

The ADP1148 uses a current-mode, constant off-time structure to switch a pair of external complementary N- and P-channel MOSFETs. The operating frequency of the device is determined by the value of the external capacitor connected to the C_T pin.

The output voltage is sensed by an internal voltage divider which is connected to the Sense(–) pin (ADP1148-3.3 and AD1148-5) or an external voltage divider returned to V_{FB} (ADP1148). A voltage comparator V, and a gain block G compare the values of the divided output voltage with a reference voltage of 1.25 V.

To maximize the efficiency, the ADP1148 automatically switches between two operational modes, power-saving and continuous. The Flip-Flop 1 is the main control element when the device is in its power-saving mode while the gain block is the main control when the output voltage moves to continuous mode. During the continuous mode of the PMOS switch on-cycle, the current comparator C, monitors the voltage between Sense(–) and Sense(+). When the voltage level reaches the threshold level, the P drive output is switched to V_{IN} which turns off the P-channel MOSFET. The timing capacitor C_T is now able to discharge at a rate determined by the off-time controller. The discharge current is made to be proportional to the value of the output voltage (measured at the Sense(–) pin) to model the inductor current which decays at a rate which is proportional to the output voltage. While the timing capacitor is discharging, the N drive output goes to V_{IN} , turning on the N-channel MOSFET. When the voltage level on the timing capacitor has discharged to the threshold voltage level V_{TH1}, comparator T switches setting Flip-Flop 1. This forces the N drive to go off and the P drive output low and subsequently turns the P-channel MOSFET on. The sequence is then repeated. As load current increases, the output voltage starts to reduce. This results in the output of the gain circuit increasing the level of the current comparator threshold, thus tracking the load current.

At very low load currents the power-saving sequence will be interrupted by the Set of Flip-Flop 2, by voltage comparator B, which also monitors the voltage across R_{SENSE}. When the load current decreases to half the designed inductor ripple current, the voltage across R_{SENSE} will reverse polarity. When this happens, comparator B will set the Q-bar output of Flip-Flop 2, which will go to logic zero state and interrupt the cycle-by-cycle operation and inhibit the output FET-driver. The output of the power supply storage capacitor will slowly be drained by the load and the output voltage starts decreasing. When this decreased voltage exceeds the V_{OS} of comparator V, this in turn will reset Flip-Flop 2, and normal cycle-by-cycle operation will resume. If the load is very small, it will take a long time for Flip-Flop 2 to reset, and during that time the oscillator capacitor may discharge below V_{TH2}. At the point at which the timing capacitor discharges below V_{TH2}, comparator S trips causing the internal sleep-bar to go low. The circuit is now in sleep mode and the N-channel Power MOSFET remains turned off. While the circuit remains in this mode, a significant amount of the circuit of the IC is turned off dropping the ground current from approximately 1.6 mA to a level of 160 µA. In this state the load current is supplied by the output capacitor. The sleep mode is also terminated by the reset of Flip-Flop 2.

To prevent both the external MOSFETs from ever being turned on simultaneously, feedback is incorporated to sense the state of the driver output pins.

Before the N drive output can go high, the P drive output must also be high. Likewise, the P drive output is unable to go low while the N drive output is high. By utilizing a constant off-time structure, the device operation is a function of the input voltage. To limit the effect of frequency variation as the device approaches dropout, the controller begins to increase the discharge current as V_{IN} drops below V_{OUT} +1.5 V. While the device is in dropout, the P-channel MOSFET is on constantly.

R_{SENSE} Selection For Output Current

The choice of R_{SENSE} is based on the required output current. The ADP1148 current comparator has a threshold range which extends from 0 mV to a maximum of 150 mV/R_{SENSE}. The current comparator threshold sets the peak of the inductor current, yielding a maximum output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current. The ADP1148 operates effectively with values of R_{SENSE} from 20 mΩ to 200 mΩ. A graph for selecting R_{SENSE} versus maximum output current is given in Figure 3. Solving for R_{SENSE} and allowing a margin for variations in the ADP1148 and external component values yields:

$$R_{SENSE} = 100\ mV/I_{MAX}$$

The peak short circuit current, ($I_{SC(PK)}$) tracks I_{MAX}. Once R_{SENSE} has been chosen, $I_{SC(PK)}$ can be predicted from the following equation:

$$I_{SC(PK)} = 150\ mV/R_{SENSE}$$

The load current, below which power-saving mode commences ($I_{POWER\text{-}SAVING}$) is determined by the offset in comparator B and the value of the inductor chosen. Comparator B is designed to have approximately 5 mV offset. This offset and the inductor can now be used to predict the power saving mode current as follows:

$$I_{POWER\text{-}SAVING} \sim 5\ mV/R_{SENSE} + V_O \times t_{OFF}/2\ L$$

The ADP1148 automatically extends t_{OFF} during a short circuit to provide adequate time for the inductor current to decay between switch cycles. The resulting ripple current causes the average short circuit current, $I_{SC(AVG)}$, to be lowered to approximately I_{MAX}.

L and C_T Selection for Operating Frequency

The ADP1148 uses a constant off-time architecture with t_{OFF} determined by an external timing capacitor C_T. Each time the P-channel MOSFET switch turns on, the voltage on C_T is reset to approximately 3.3 V. During the off time, C_T is discharged by a current which is proportional to V_{OUT}. The voltage on C_T is analogous to the current in inductor L, which likewise decays at a rate proportional to V_{OUT}. Therefore, the inductor value must track the timing capacitor value.

The value of C_T is calculated from the preferred continuous mode operating frequency:

$$C_T = 1/2.6 \times 10^4 \times f$$

Assumes V_{IN} = 2 V_{OUT} (Figure 1 circuit).

A graph for selecting C_T versus frequency including the effects of input voltage is given in Figure 5.

*Component, voltage, current, etc., values are in SI-units (international standard) unless otherwise indicated.

As the operating frequency is increased, the gate charge losses will cause reduced efficiency (see Efficiency section). The full formula for operating frequency is given by:

$$f = (1 - V_{OUT}/V_{IN})/t_{OFF}$$

where $t_{OFF} = 1.3 \times 10^4 \times C_T \times V_{REG}/V_{OUT}$.

V_{REG} is the desired output voltage (i.e., 5 V or 3.3 V), V_{OUT} is the measured output voltage. Thus, $V_{REG}/V_{OUT} = 1$ in regulation.

Note that as V_{IN} reduces, the frequency also decreases. When the input to output voltage differential drops below 1.5 V, the ADP1148 reduces t_{OFF} by increasing the discharge current in C_T. This prevents audible operation before the device goes into dropout.

Once the frequency has been set by C_T, the inductor L must be chosen to provide no more than 25 mV/R_{SENSE} of peak-to-peak inductor ripple current. This is set by the equation:

$$\frac{25\ mV}{R_{SENSE}} = \frac{V_{OUT} \times t_{OFF}}{L_{MIN}}$$

or

$$L_{MIN} = \frac{V_{OUT} \times t_{OFF} \times R_{SENSE}}{25\ mV}$$

Substituting for t_{OFF} from above gives the minimum required inductor value of:

$$L_{MIN} = 5.1 \times 10^5 \times R_{SENSE} \times C_T \times V_{REG}$$

As the inductor value increases above the minimum value, the ESR requirements for the output capacitor are relaxed at the expense of efficiency. If too small an inductor is used, the inductor current will decrease past zero and change polarity. A result of this occurrence will be that the ADP1148 may not be in power saving mode operation and efficiency will be significantly reduced at low currents.

Inductor Core

Once the minimum value for L is known, the selection of the inductor must be made. High efficiency converters generally cannot accommodate the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy (MPP), or "Kool Mμ "®cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss, so design goals can focus on copper loss and preventing saturation. Ferrite core material saturates "hard," which causes the inductance to collapse abruptly when the peak design current is exceeded. This results in a sharp increase in inductor ripple current and subsequently output voltage ripple which can cause the power saving mode operation to be falsely triggered in the ADP1148. To prevent this action from occurring, do not allow the core to saturate!

Molypermalloy from Magnetics, Inc., is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is "Kool Mμ". Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. Many new designs for surface mount components are also available from Coiltronics which do not increase the component height significantly.

Power MOSFET

Two external power MOSFETs must be selected for use with the ADP1148, a P-channel MOSFET for the main switch, and an N-channel MOSFET for the synchronous switch. The main selection parameters for the power MOSFETs are the threshold voltage $V_{GS(TH)}$ and on resistance $R_{DS(ON)}$.

The minimum input voltage dictates whether standard threshold or logic-level threshold MOSFETs must be used. For $V_{IN} > 8$ V, standard threshold MOSFETs ($V_{GS(TH)} < 4$ V) may be used. If V_{IN} is expected to drop below 8 V, logic-level threshold MOSFETs ($V_{GS(TH)} < 2.5$ V) are strongly recommended. When logic-level MOSFETs are used, the ADP1148 supply voltage must be less than the absolute maximum V_{GS} rating for the MOSFETs (e.g., >±8 V of IRF7304.

The maximum output current I_{MAX} determines the $R_{DS(ON)}$ requirement for the two power MOSFETs. When the ADP1148 is operating in continuous mode, the simplifying assumption can be made that one of the two MOSFETs is always conducting the average load current. The duty cycles for the MOSFET and diode are given by:

$$P\text{-}Channel\ Duty\ Cycle = V_{OUT}/V_{IN}$$

$$N\text{-}Channel\ Duty\ Cycle = (V_{IN} - V_{OUT})/V_{IN}$$

From the duty cycle the required $R_{DS(ON)}$ for each MOSFET can be derived:

$$P\text{-}Ch\ R_{DS(ON)} = (V_{IN} \times P_P)/[V_{OUT} \times I_{MAX}^2 \times (1 + d_P)]$$

$$N\text{-}Ch\ R_{DS(ON)} = (V_{IN} \times P_N)/[(V_{IN} - V_{OUT}) \times I_{MAX}^2 \times (1 + d_N)]$$

where P_p and P_N are the allowable power dissipations and d_p and d_N are the temperature dependency of $R_{DS(ON)}$. P_P and P_N will be determined by efficiency and/or thermal requirements (see Efficiency). (1+d) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs. temperature curve, but d = 0.007/°C can be used as an approximation for low voltage MOSFETs.

The Schottky diode D1 shown in Figure 1 conducts only during the deadtime between the conduction of the two power MOSFETs. D1's purpose is to prevent the body-diode of the N-channel MOSFET from turning on and storing charge during the dead time, which could cost as much as 1% in efficiency. D1 should be selected for forward voltage of less than 0.5 V when conducting I_{MAX}.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{required} \quad I_{RMS} \sim [V_{OUT}(V_{IN} - V_{OUT})]^{0.5} \times I_{MAX}/V_{IN}$$

This formula has a maximum at $V_{IN} = 2\ V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the

design. Always consult the manufacturer if there is any question. An additional 0.1 µF – 1 µF ceramic bypass capacitor is advised on V_{IN} Pin 3 parallel with C_{IN}. The selection of C_{OUT} is driven by the required effective series resistance (ESR). The ESR of C_{OUT} must be less than twice the value of R_{SENSE} for proper operation of the ADP1148:

$$C_{OUT} \text{ required } ESR < 2\, R_{SENSE.}$$

Optimum efficiency is obtained by making the ESR equal to R_{SENSE}. As the ESR is increased up to 2 R_{SENSE}, the efficiency degrades by less than 1%.

Manufacturers such as Sprague, and United Chemmicon should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor has the lowest ESR for its size, at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface-mount applications multiple capacitors may have to be paralleled to meet the capacitance, ESR, or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface-mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. Consult the manufacturer for other specific recommendations. The C_O output filter capacitor has to be sized correctly to avoid excessive ripple voltages at low frequencies. See Figure 5 for output capacitor selection.

Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in dc (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $DI_{LOAD} \times ESR$, where *ESR* is the effective series resistance of $C_{OUT.}$ DI_{LOAD} also begins to charge or discharge C_{OUT} until the regulator loop adapts to the current change and returns V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem. The external components on the I_{TH} pin shown in the Figure 1 circuit will prove adequate compensation for most applications.

A second, more severe transient is caused by switching in loads with large (>1 mF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the inrush current to these capacitors below the current limit of the circuit.

Efficiency

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%\ Efficiency = 100\% - (L1 + L2 + L3 + \ldots)$$

where *L*1, *L*2, etc. are the individual losses as a percentage of input power (For high efficiency circuits only small errors are incurred by expressing losses as a percentage of output power.).

Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in ADP1148 circuits:

1) ADP1148 dc bias current,
2) MOSFET gate charge currents,
3) $I^2 \times R$ losses.

1) The dc supply current is the current which flows into V_{IN} Pin 3 less the gate charge current. For $V_{IN} = 10\ V$ the ADP1148 dc supply current is 160 µA for no load, and increases proportionally with load up to a constant 1.6 mA after the ADP1148 has entered continuous mode. Because the dc bias current is drawn from V_{IN}, the resulting loss increases with input voltage. For $V_{IN} = 10\ V$ the dc bias losses are generally less than 1% for load currents over 30 mA. However, at very low load currents the dc bias current accounts for nearly all of the loss.

2) MOSFET gate charge currents result from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} which is typically much larger than the dc supply current. In continuous mode, $I_{GATECHG} = f\,(Q_P + Q_N)$. The typical gate charge for a 100 mΩ N-channel power MOSFET is 25 nC and for the P-channel about twice that value. This results in $I_{GATECHG} = 7.5\ mA$ in 100 kHz continuous operation for a 2% to 3% typical midcurrent loss with $V_{IN} = 10$ V.

   Note that the gate charge loss increases directly with both input voltage and operating frequency. This is the principal reason why the highest efficiency circuits operate at moderate frequencies. Furthermore, it argues against using a larger MOSFET than necessary to control $I^2 \times R$ losses.

3) $I^2 \times R$ losses are easily predicted from the dc resistances of the MOSFET, inductor, and current shunt. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the P-channel and N-channel MOSFETs. If the two MOSFETs have about the same $R_{DS(ON)}$, the resistance of one MOSFET can be simply summed with the resistances of L and R_{SENSE} to obtain $I^2 \times R$ losses. For example, if each $R_{DS(ON)}$ = 100 mΩ, R_L = 150 mΩ, and R_{SENSE} = 50 mΩ, then the total resistance is 300 mΩ. This results in losses ranging from 3% to 10% as the output current increases from 0.5 A to 2 A. $I^2 \times R$ losses cause the efficiency to roll-off at high output currents.

Figure 6 shows how the efficiency losses in a typical ADP1148 regulator. The gate charge loss is responsible for the majority of the efficiency lost in the midcurrent region. If power saving mode operation was not employed at low currents, the gate charge loss alone would cause the efficiency to drop to unacceptable levels. With power saving mode operation, the dc supply current represents the lone (and unavoidable) loss component which continues to become a higher percentage as output current is reduced. As expected, the $I^2 \times R$ losses dominate at high load currents. Other losses including C_{IN} and C_{OUT} ESR dissipative losses, MOSFET switching losses, Schottky conduction losses during deadtime and inductor core losses, generally account for less than 2% total additional loss.

Design Example

As a design example, assume V_{IN} = 12 V (nominal), V_{OUT} = 5 V, I_{MAX} = 2 A, and f = 200 kHz, R_{SENSE}. C_T, and L can immediately be calculated:

$$R_{SENSE} = 100\ mV/2 = 50\ m\Omega$$

$$t_{OFF} = (1/200\ kHz) \times [1 - (5/12)] = 2.92\ \mu S$$

$$C_T = 2.92\ \mu S/(1.3 \times 10^4) = 220\ pF$$

$$L\ min = 5.1 \times 10^5 \times 50\ E\text{-}3\ \Omega \times 220\ pF \times 5\ V = 28\ \mu H$$

Assume that the MOSFET dissipations are to be limited to $P_N = 2P_P$ = 250 mW.

If T_A = 50°C and the thermal resistance of each MOSFET is 50°C/W, then the junction temperatures will be 63°C and d_P = d_P = 0.007 × (63–25) = 0.27.

The required $R_{DS(ON)}$ for each MOSFET can now be calculated:

$$P\text{-}Ch\ R_{DS(ON)} = 12 \times 0.25/5 \times 2 \times 1.27 = 120\ m\Omega$$

$$N\text{-}Ch\ R_{DS(ON)} = 12 \times 0.25/7 \times 2 \times 1.27 = 85\ m\Omega$$

The P-channel requirement can be met by a IRF7204. The N-channel requirement can be met by a IRF7404. Note that the most stringent requirement for the N-channel MOSFET is with V_{OUT} = 0 (i.e., short circuit). During a continuous short circuit, the worst case N-channel MOSFET dissipation rises to:

$$P_N \sim I_{SC(AVG)}{}^2 \times R_{DS(ON)} \times (1 + d_N)$$

With the 50 mΩ sense resistor $I_{SC(AVG)}$ = 2 A will result, increasing the N-channel dissipation to 0.45 W at die temperature of 73°C.

C_{IN} will require an rms current rating of at least 1 A at temperature, and C_{OUT} will require an ESR of 50 mΩ for optimum efficiency.

Now allow V_{IN} to drop to its minimum value. At lower input voltages, the operating frequency will decrease and the P-channel will be conducting most of the time causing the power dissipation to increase. At $V_{IN(MIN)}$ = 7 V, the frequency shifts to:

$$f_{MIN} = (1 - V_{OUT}/V_{IN})/t_{OFF} = (1/2.92\ \mu s) \times (1 - 5/7) = 98\ kHz$$

and the P-channel power dissipation increases to:

$$P_P = (120\ m\Omega)\ (2\ A)^2\ (1.27)\ 5\ V/7\ V = 435\ mW$$

This last step is needed to ensure the maximum temperature of the P-channel MOSFET is not exceeded.

ADP1148 Adjustable Applications

When an output voltage other than 3.3 V or 5 V is required, the ADP1148 adjustable version is used with an external resistive divider from V_{OUT} to V_{FB} Pin 9. The regulated voltage is determined by:

$$V_{OUT} = 1.25\ (1 + R2/R1)$$

To prevent a stray pickup, a 100 pF capacitor is suggested across R1 located close to the ADP1148.

Auxiliary Windings

The ADP1148 synchronous switch removes the normal limitation that power must be drawn from the inductor primary winding in order to extract power from auxiliary windings. With synchronous switching, auxiliary outputs may be loaded without regard to the primary output load, providing that the loop remains in continuous mode operation.

Output Crowbar

An added feature to using an N-channel MOSFET as the synchronous switch is the ability to crowbar the output with the same MOSFET. Pulling the timing cap C_T pin above 1.5 V when the output voltage is greater than the desired regulated value will turn "on" the N-channel MOSFET and turn "off" the P-channel MOSFET.

A fault condition such as an external short between V_{IN} and V_{OUT}, or an internal short of the P-channel device which causes the output voltage to go above a maximum allowable value can be detected by external circuity. Turning on the N-channel MOSFET when this fault is detected will cause large currents to flow and blow the system fuse.

The N-channel MOSFET needs to be sized so it will safely handle this over current condition. The typical delay from pulling the C_T pin high and the N drive, Pin 14 going high is 250 ns. Note: under shutdown conditions, the N-channel MOSFET is held OFF and pulling the C_T pin high will not cause the N-channel MOSFET to crowbar the output.

A simple N-channel FET can be used as an interface between the overvoltage detect circuitry and the ADP1148 as shown in Figure 16.

Troubleshooting

Since efficiency is critical to ADP1148 applications, it is very important to verify that the circuit is functioning correctly in both continuous and power saving mode operation. The waveform to monitor is the voltage on the timing capacitor C^T pin.

In continuous mode ($I_{LOAD} > I_{POWER\ SAVING\ MODE}$), the voltage on the C_T pin should be a sawtooth with a 0.9 V p-p swing. This voltage should never dip below 2 V as shown in Figure 8a.

When load currents are low ($I_{LOAD} < I_{POWER\ SAVING\ MODE}$), power saving mode operation occurs. The voltage on the C_T pin now falls to ground for periods of time as shown in Figure 8b. If the C_T pin is observed falling to ground at high output currents, it indicates poor decoupling or improper grounding. Refer to the Board Layout list.

Board Layout

When laying out the printed circuit board, the following check list should be used to ensure proper operation of the ADP1148. These items are also illustrated graphically in the layout diagram of Figure 18. Check the following in your layout:

1) Are the signal and power grounds segregated? The ADP1148 SIGNAL GND (Pin 11) must return to the (–) plate of C_{OUT}. The power ground returns to the source of the N-channel MOSFET, anode of the Schottky diode, and (–) plate of C_{IN}, which should have as short lead lengths as possible.
2) Does the ADP1148 SENSE(–), (Pin 7), connect to a point close to R_{SENSE} and the (+) plate Of C_{OUT}? In adjustable versions the resistive divider R1, R2 must be connected between the (+) plate of C_{OUT} and signal ground.
3) Are the SENSE(–) and SENSE(+) leads routed together with minimum PC trace spacing? The 1000 pF capacitor between Pins 7 and 8 should be as close as possible to the ADP1148.
4) Does the (+) plate of C_{IN} connect to the source of the P-channel MOSFET as closely as possible? This capacitor provides the ac current to the P-channel MOSFET.
5) Is the input decoupling capacitor (1 µF) connected closely between V_{IN} (Pin 3) and POWER GND (Pin 12)? This capacitor carries the MOSFET driver peak currents.
6) Is $INTV_{CC}$ (Pin 5) decoupled with a 10 nF capacitor to signal ground?
7) Is the SHUTDOWN (Pin 10) actively pulled to ground during normal operation? The Shutdown pin is high impedance and must not be allowed to float.

To prevent noise spikes from erroneously tripping the current comparator, a 1000 pF capacitor is needed across Sense(–) and Sense(+).

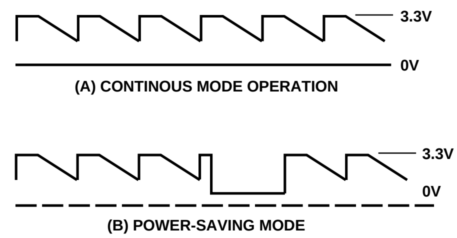


Figure 17. C_T Waveforms

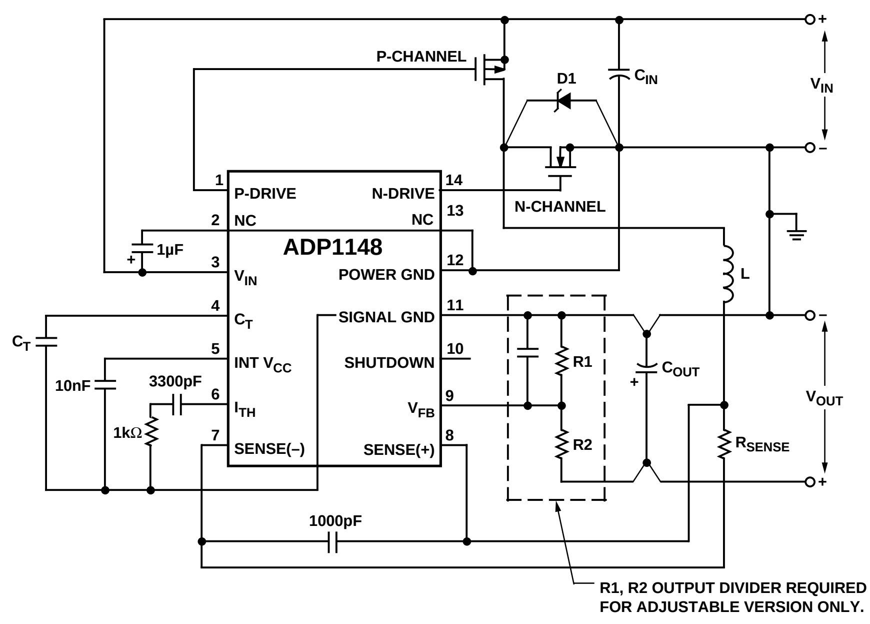


Figure 18. ADP1148 Layout Diagram (See Board Layout)

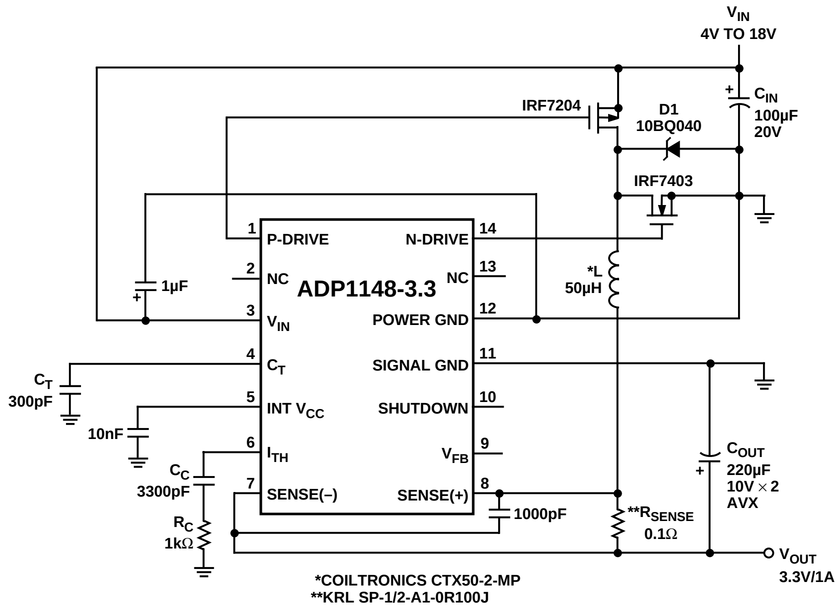


Figure 19. ADP1148 Low Dropout, 3.3 V/1 A High Efficiency Regulator

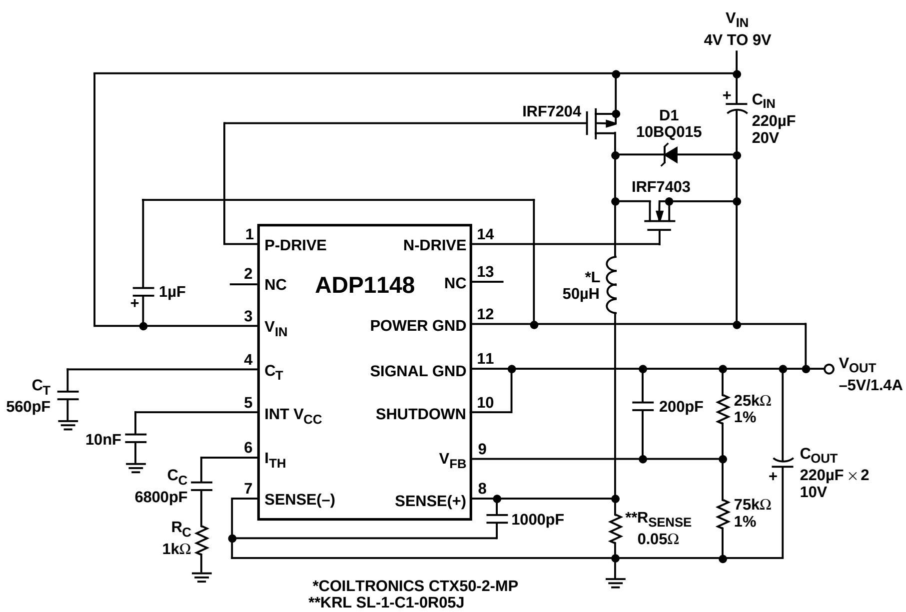


Figure 20. 4 V to 9 V Input Voltage to –5 V/1.4 A Regulator

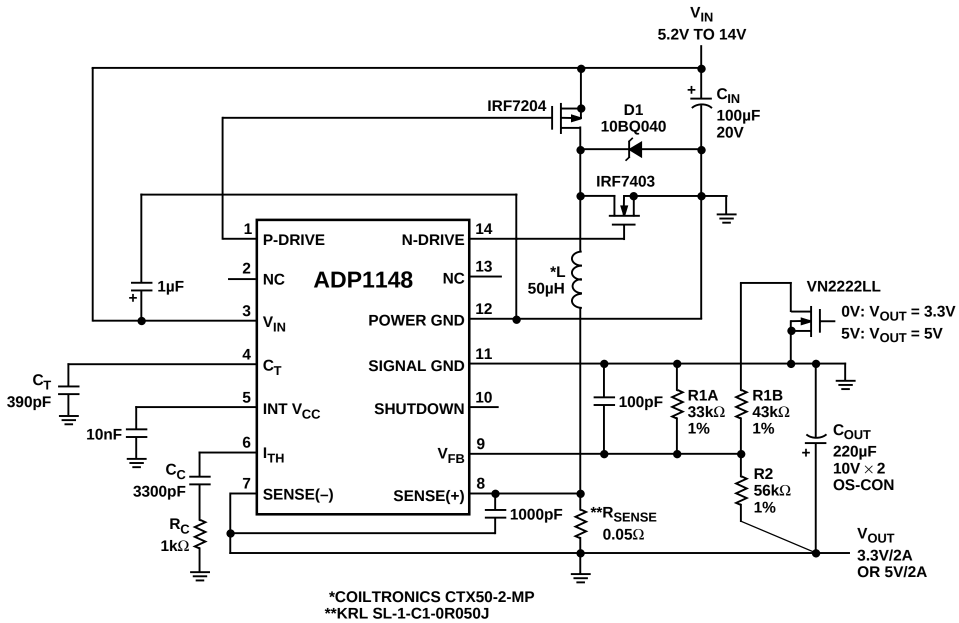
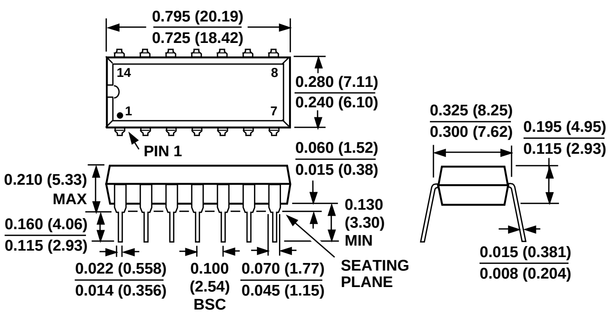


Figure 21. Logic Selectable 5 V/1 A or 3.3 V/2 A High Efficiency Regulator

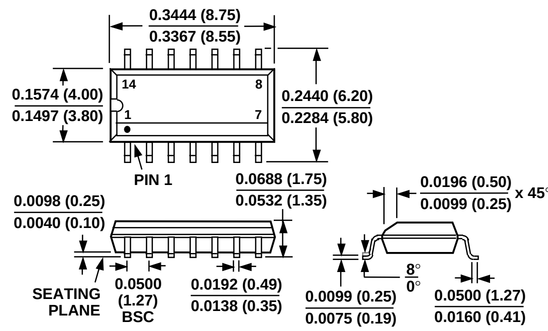
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead Plastic DIP (N-14)



14-Lead Plastic SO (SO-14)



C2219–12–10/96

PRINTED IN U.S.A.